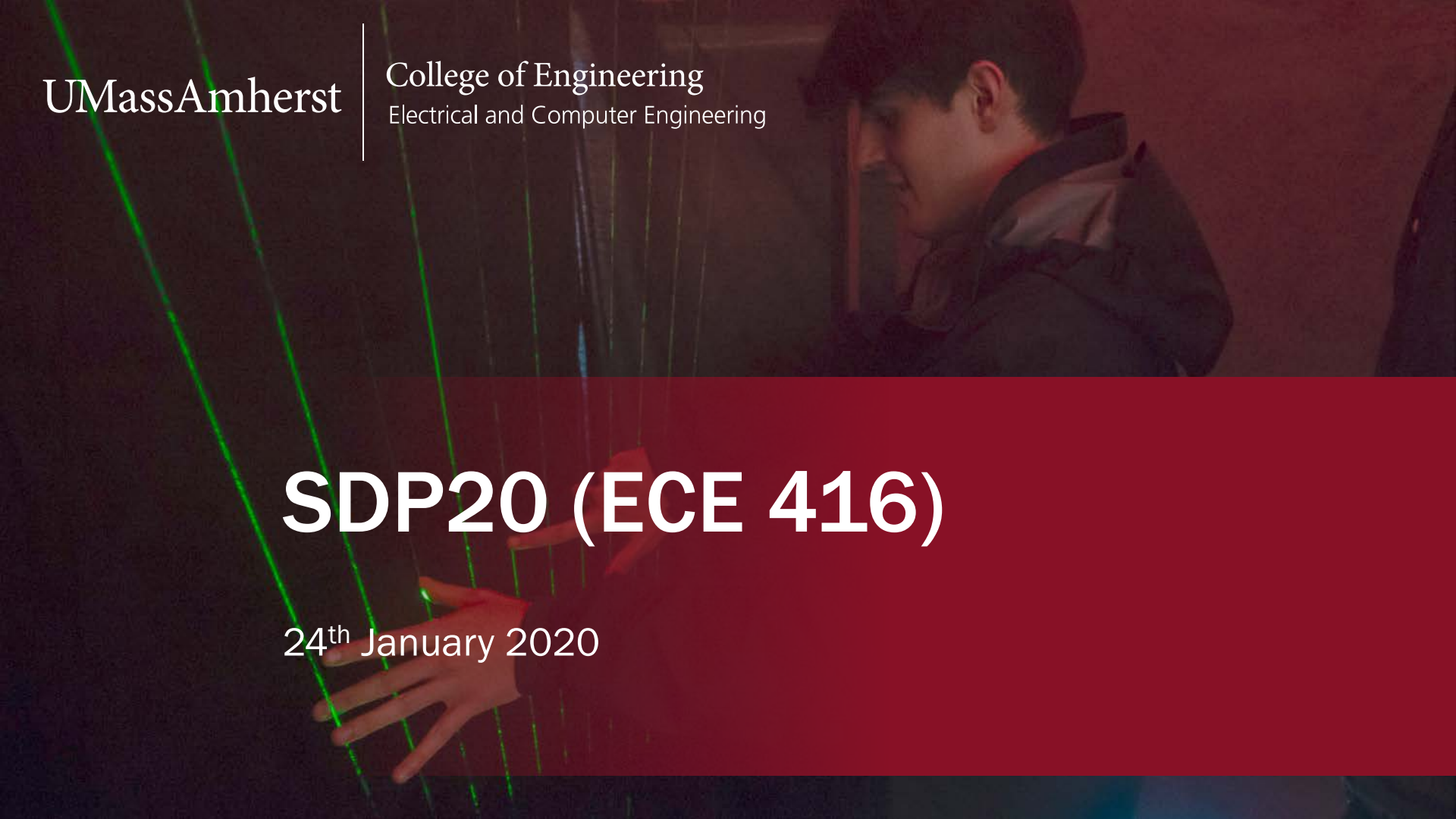

UMassAmherst

College of Engineering
Electrical and Computer Engineering

SDP20 (ECE 416)

24th January 2020

Schedule

January 2020

Sun	Mon	Tue	Wed	Thu	Fri	Sat
			1	2	3	4
5	6	7	8	9	10	11
12	13	14 MDR Reports returned	15	16	17	18
19	20	21 First Day of Classes	22	23	24 Lecture	25
26	27 Benchsides	28 Revised MDR Reports due	29 Benchsides	30	31 Benchsides	1

February 2020

Sun	Mon	Tue	Wed	Thu	Fri	Sat
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17 Holiday	18 Monday Schedule	19	20	21	22
23	24 Benchsides	25	26 Benchsides	27	28 Benchsides	29

March 2020

Sun	Mon	Tue	Wed	Thu	Fri	Sat
1	2	3	4	5	6	7
8	9 CDR	10 CDR	11 CDR	12 CDR	13 CDR	14
15	16 Spring Break begins	17	18	19	20 Spring Break ends	21
22	23	24	25	26	27	28
29	30	31				

April 2020

Sun	Mon	Tue	Wed	Thu	Fri	Sat
			1	2	3	4
5	6 Benchsides	7	8 Bnchsides	9	10 Benchsides	11
12	13 FPR	14 FPR	15 FPR	16 FPR	17 FPR	18
19	20 Holiday	21	22 Monscheduleday schedule	23	24 SDP Demo Day (10am-2pm)	25 SDP Demo Day (noon-4pm)
26	27	28	29 Last day of classes	30	1 ECE Banquet	2

May 2020

Sun	Mon	Tue	Wed	Thu	Fri	Sat
					1 ECE Banquet	2
3	4	5	6	7 Last Day of Exams	8 UG Commencement	9 COE Graduation
10	11 Final Report Due	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30

MDR report comments

1) Teams 2, 6, 12, 14, 18 and 22 reports are good examples of structure, technical content, organization and writing. Please see their reports posted on the websites, and please post your reports on team websites.

2) Common feedback on reports:

a) Provide citations to the data sheets and/or websites for all major components – both SW and HW.

b) Refer to, and discuss all figures and tables in the text.

c) Please consider providing a SW flow diagram of your project. Together with the block diagram, they are the most important design figures of the report – they convey much.

Team 6

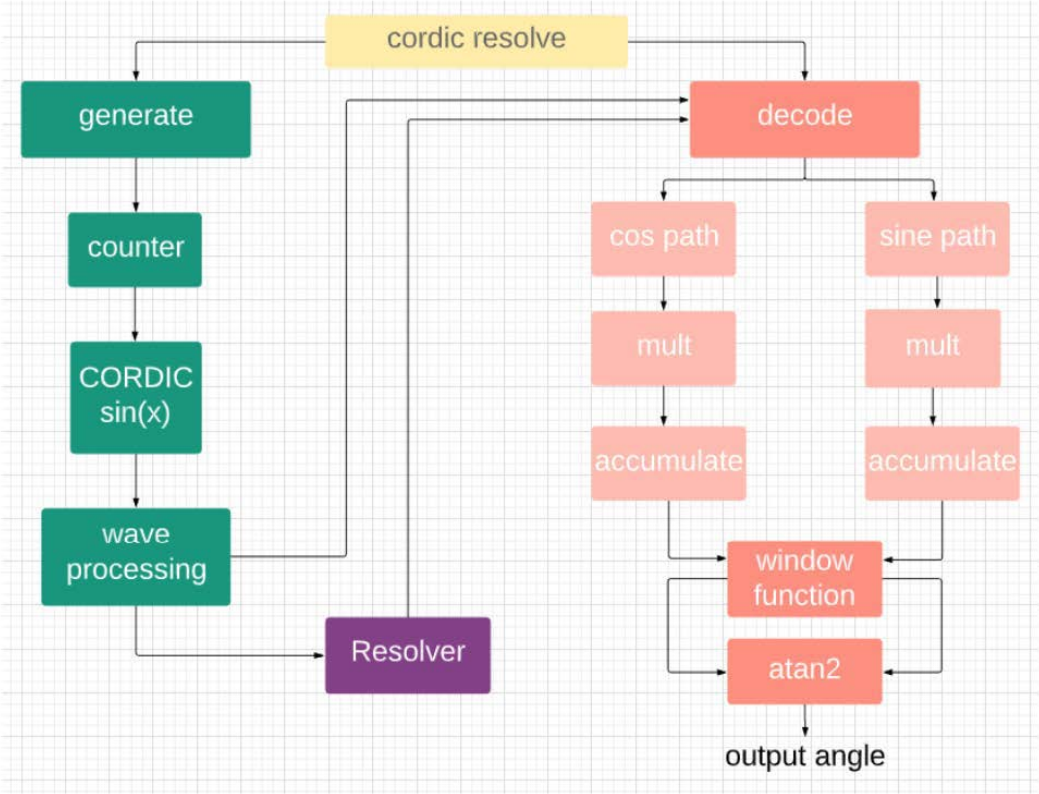

Figure 4: Verilog hierarchy of generate and decode modules within the FPGA.

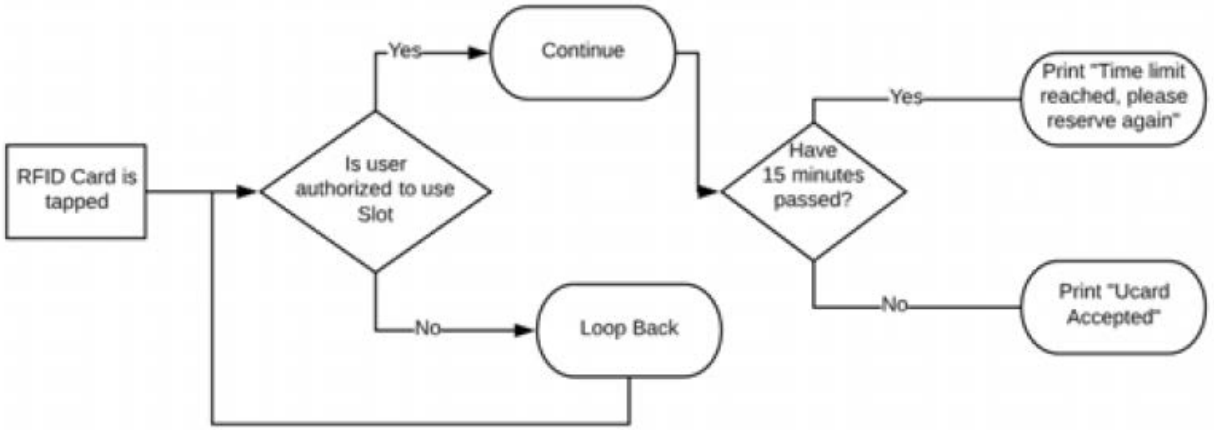

Figure 2: User ID Control Diagram. How our backend software manipulates user data

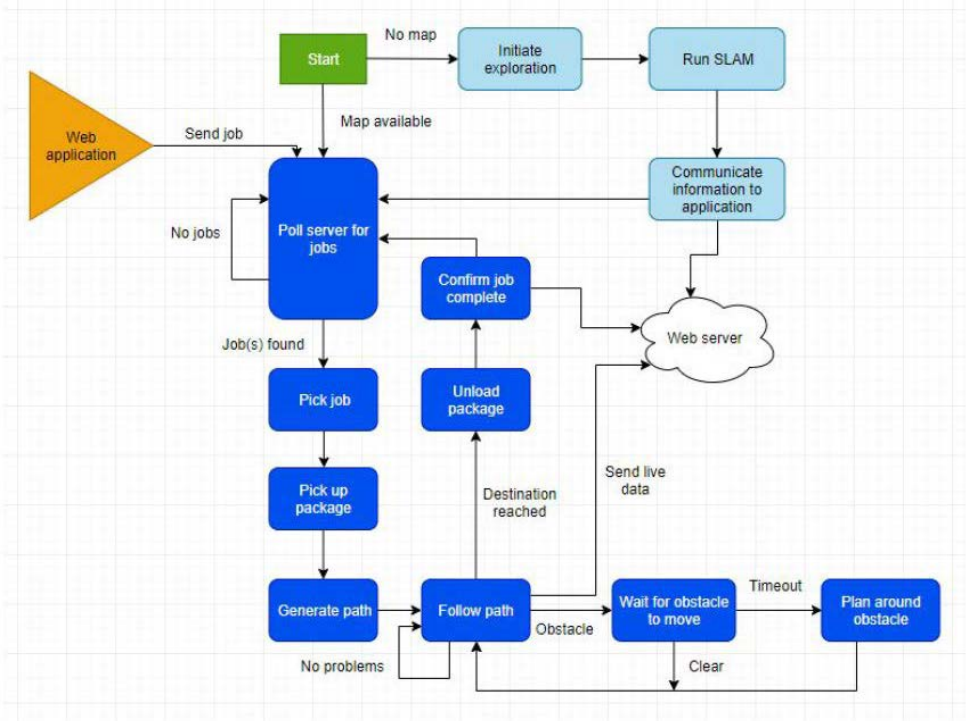

Figure 2: A state machine representing the program flow of our robot, including nodes for our stretch goals.

Progression

- MDR (functioning prototype)
- CDR (functioning product)
- FPR (final product)

MDR → CDR

- Electronic: design, fabrication and troubleshooting PCBA
- Mechanical: design and fabrication enclosures
- Specifications: testing, data analysis, redesign

Benchsides

Benchside Meeting			Benchside Meeting			Benchside Meeting	
Mon 27th Jan 2020			Wed 29th Jan 2020			Fri 31st Jan 2020	
location: SDP lab			location: SDP lab			location: SDP lab	
Time (pm)	Team		Time (pm)	Team		Time (pm)	Team
4:00	Team 13		4:00	~~Team 23~~ Team 18		4:00	Team 16
4:15	Team 11		4:15	Team 24		4:15	Team 27
4:30	Team 17		4:30	Team 9		4:30	Team 8
4:45	~~Team 18~~ Team 23		4:45	Team 2		4:45	Team 7
5:00	Team 6		5:00	Team 10		5:00	Team 15
5:15	Team 21		5:15	Team 25		5:15	Team 20
5:30	Team 19		5:30	Team 14		5:30	~~Team 3~~ Team 5
5:45	Team 4		5:45	~~Team 5~~ Team 3		5:45	Team 1
6:00	Team 26		6:00	Team 12		6:00	Team 22

Swaps

-
-
-

Volunteers: SDP20 Demos @ OpenHouses

- Sunday, 23rd February
- Sunday, 15th March

Discussion?

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College of Engineering

Electrical and Computer Engineering

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